Integration & Test

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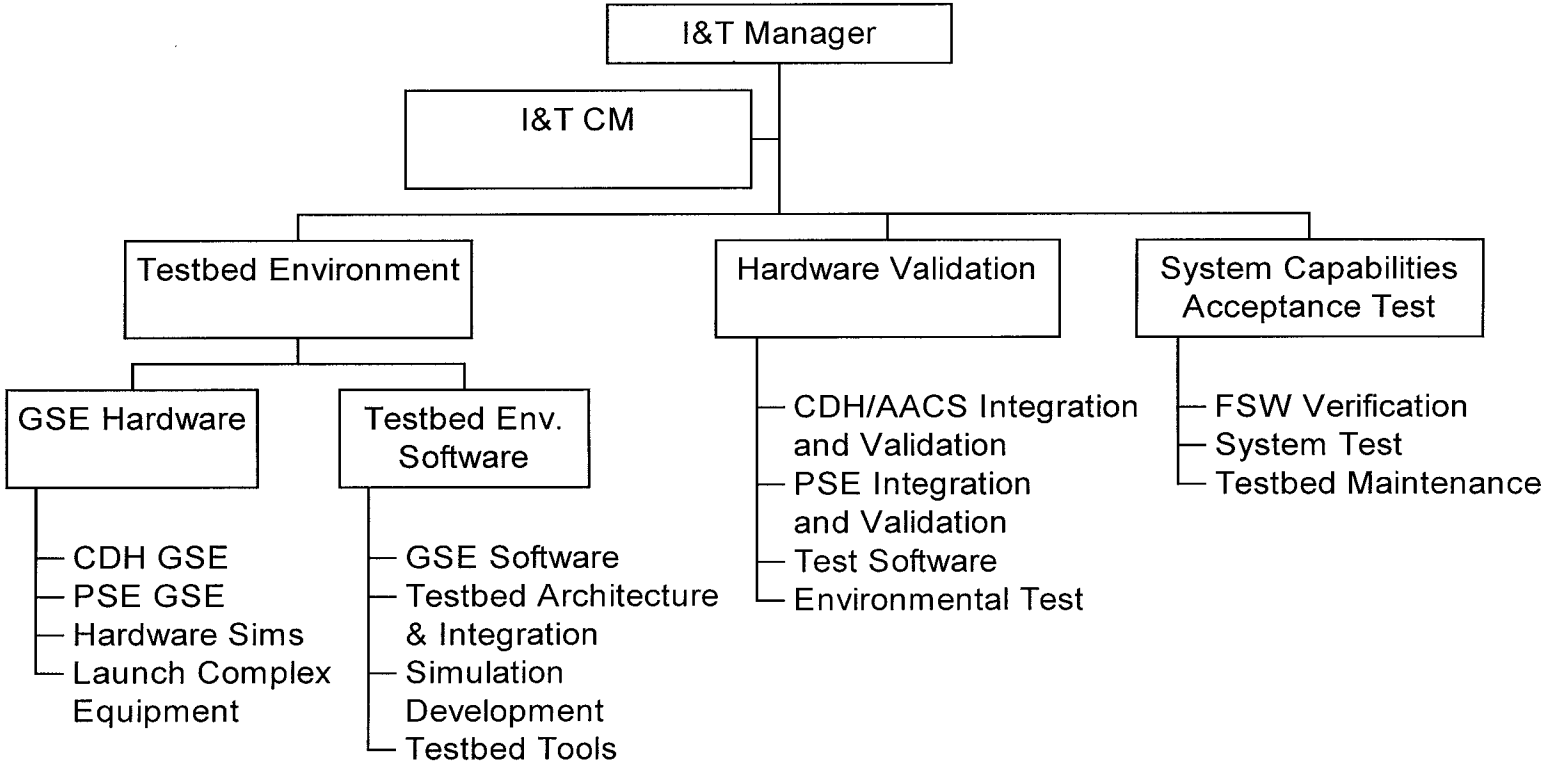
Organization Chart

Europa Orbiter Avionics
Integration and Test



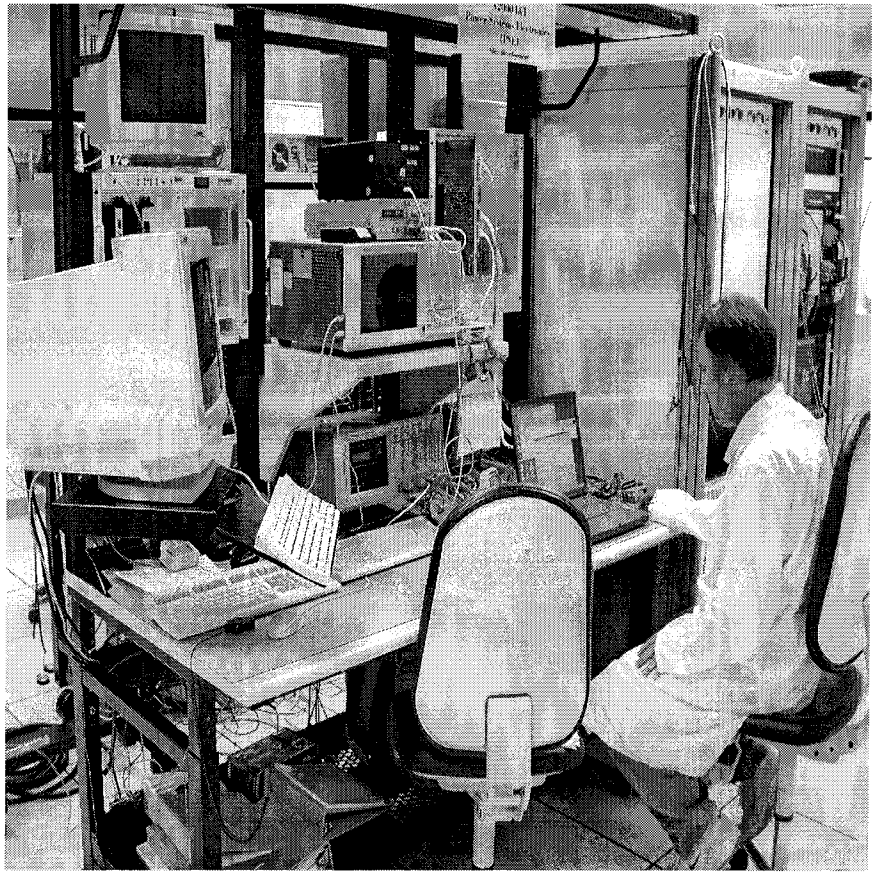
Hardware Verification Test Scope

- Acceptance test vendor supplied hardware and integrate into avionics chassis
  - Concentrate on interfaces
- Perform detailed slice checkout of JPL-supplied hardware and integrate into avionics chassis
- Develop test software to functionally verify slices and avionics system
- Validate system, subsystem, and assembly hardware requirements
- Perform avionics margin and characterization tests

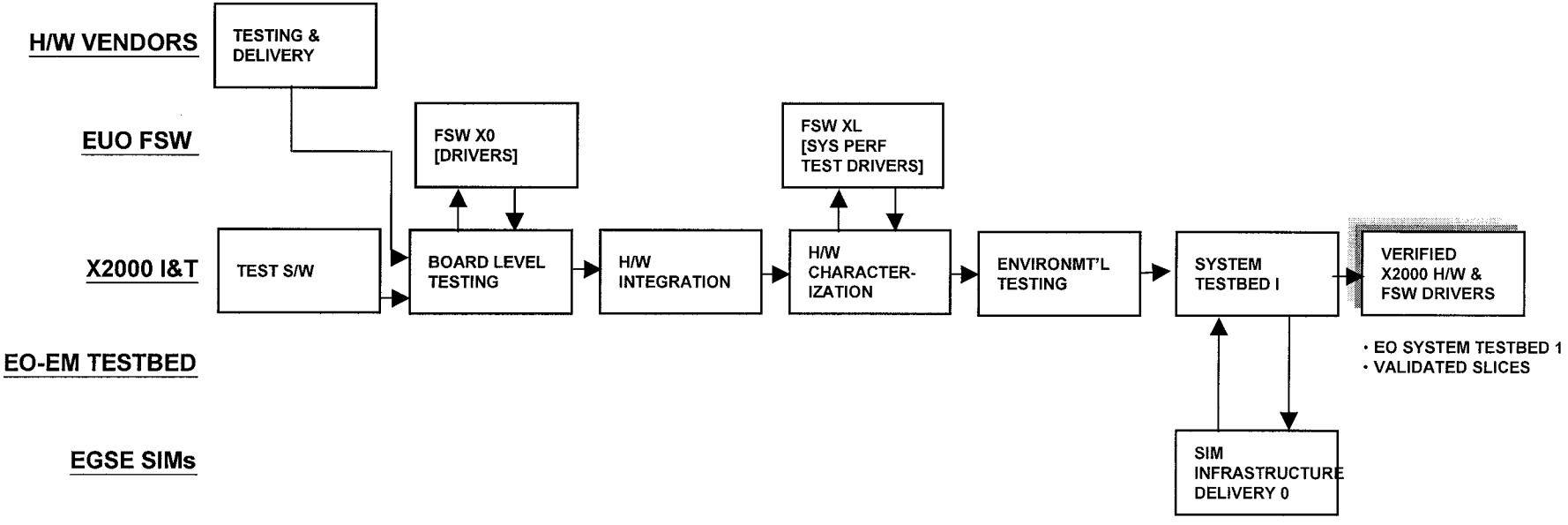
Hardware Verification Test Scope

- Perform environmental qualification and flight acceptance tests
- Integrate and deliver three test beds
  - Verify each unique configuration
  - Deliver integrated product (includes GSE, avionics, cabling, test software, test documentation)
- Develop test documentation (Plans, Specifications, Procedures, Reports)
- Provide test bed maintenance and support

Hardware Verification Lab Photos



X2000 AVIONICS H/W FLOW w/ FSW DRIVERS (PHASE I)



Test Flow and Definition - Part 1

- Vendor-Supplied Slice Tests
  - Perform acceptance tests using vendor supplied support equipment and procedures
    - Assume detailed slice checkout has been performed by Vendor
    - Maintain capability to test slice in case there are any anomalies throughout test flow
- JPL-Supplied Slice Tests
  - Perform detailed internal slice checkout
    - Use JPL developed Bench Checkout Equipment
    - Develop test software to perform tests
    - Verify slice functional requirements
    - Perform bus validation tests

Test Flow and Definition - Part 2

- Slice - to - Slice Integration
  - Starts once two unique slices are available to integrate into chassis
  - Assumes detailed internal slice validation is complete
  - Emphasizes interface checkout / interactions
    - Real hardware interface now replaces simulators
  - Starts GSE integration effort

Test Flow and Definition - Part 3

- Subsystem Build-Up
  - Continue to add slices and verify interfaces until complete
    - Can deliver partial capability to test beds
    - Can build up each node in parallel if needed to gain schedule
      - GSE partitioning allows CDH and PSE testing to be split
      - GSE schedule also allows CDH nodes to be tested in parallel
  - Perform margin and characterization tests
- Avionics Systems Tests
  - Perform bus characterization and system performance tests
  - Perform final requirements validation
  - Perform integrated HW / FSW validation tests
  - Integrate telecom, ACS sensors, and instruments

Requirements Evaluation

- The complete hardware validation test matrix will be a key product deliverable to each test bed
- The test matrix will be the focus of each test specification
  - Each requirement will be evaluated for testability, test phase, and test method
  - Each test defined will drive GSE, TSW, and specialty test equipment requirements / capabilities
- Completed test matrices will include test reference data (analysis memos, test software modules, test procedures, and test reports)

Ground Support Equipment Features

- Blends what has traditionally been 3 separate GSE sets: ACS, CDH, Power
- Architecture supports real time HW in the loop testing - expandable capability
- Significant GSE SW heritage
- Multi-purpose, one design, concept
  - Standalone Power Subsystem Integration and test
  - Standalone CDH integration and test
  - Launch Complex Equipment
- Heavy reliance on GDS

Current Status

- Slice Verification
  - Performed acceptance tests on the following vendor slices
    - NVM, SFC, TAS
  - Performed functional verification of the following JPL-developed slices
    - SIO verification almost complete
      - Verified I2C, UART, Custom Logic, Discretes, PCI - 100%
      - 1394 verification in process - detailed backup material available
    - SIA verification in process
      - All functional interfaces have been verified
      - Detailed checkout in process
    - TIF verification complete

STB = System Testbed

Current Status

- Integration Tests
  - SFC to SIO and SIA through EM backplane
  - SIO to TAS across I2C bus
- Testbed Development
  - Delivered STB-1 Phase 1 (9/00)
    - Single string CDH
    - Used for FSW Driver integration on hardware platform
  - Building up STB-1 Phase 2 (11/01)
    - Dual string CDH
    - Will be used for FSW performance tests
  - Engineering Model testbed STB-2 to be completed 11/02

1394 Verification Progress

Backup Material

1394 Cables

- Flight configuration verified against 1394 specification
  - Cable configuration tested against 1394 cable specification and meet the 100Mhz requirements
    - Controlled impedance flight cable developed using materials that meet the space and high radiation requirements
    - Matched impedance connectors designed using materials that meet the space and high radiation requirements
- Connectors redesigned to withstand longer thermal cycling

SL763 Hardware and HAL Software

- Hardware implementation of the 1394 link layer with status bits in registers
  - Operational verification of register status bits for nominal and error cases per vendor documentation and the 1394 specification
  - 91 functions encompassed in 25 registers
- Software and hardware implementation of the 1394 Transaction layer using status bit in the hardware
  - Operational verification of register status bits for nominal and error cases per vendor documentation and 1394 specification
  - 99 functions encompassed in 21 registers
- Software implementation of the 1394 Serial Bus layer
  - Self ID and Tree ID process verified
- Hardware Abstraction Layer (HAL) software incorporated into flight software
  - HAL software modified for robust space application
  - Flight software being used to verify 1394 functionality and hardware performance

1394 Bus Functionality Verification

- Asynchronous Transfers
  - Successful reads and writes of data payloads of up to 512 bytes in single cycle verified
- Isochronous Transfers
  - Successful transmissions of up to 1024 bytes in single cycle verified
- Asynchronous and Isochronous Transfers
  - Successful Asynchronous transfer with a payload of 512 bytes and Isochronous transfer with a payload of 1024 bytes in single cycle
- Illegal Transfers
  - Illegal transfers detected by hardware and software protection schemes
- DMA transfers to local memory via PCI Bus
  - Automatic DMA transfers of data and commands using PCI bus
- Memory protection
  - Software and hardware memory protection schemes proven and verified